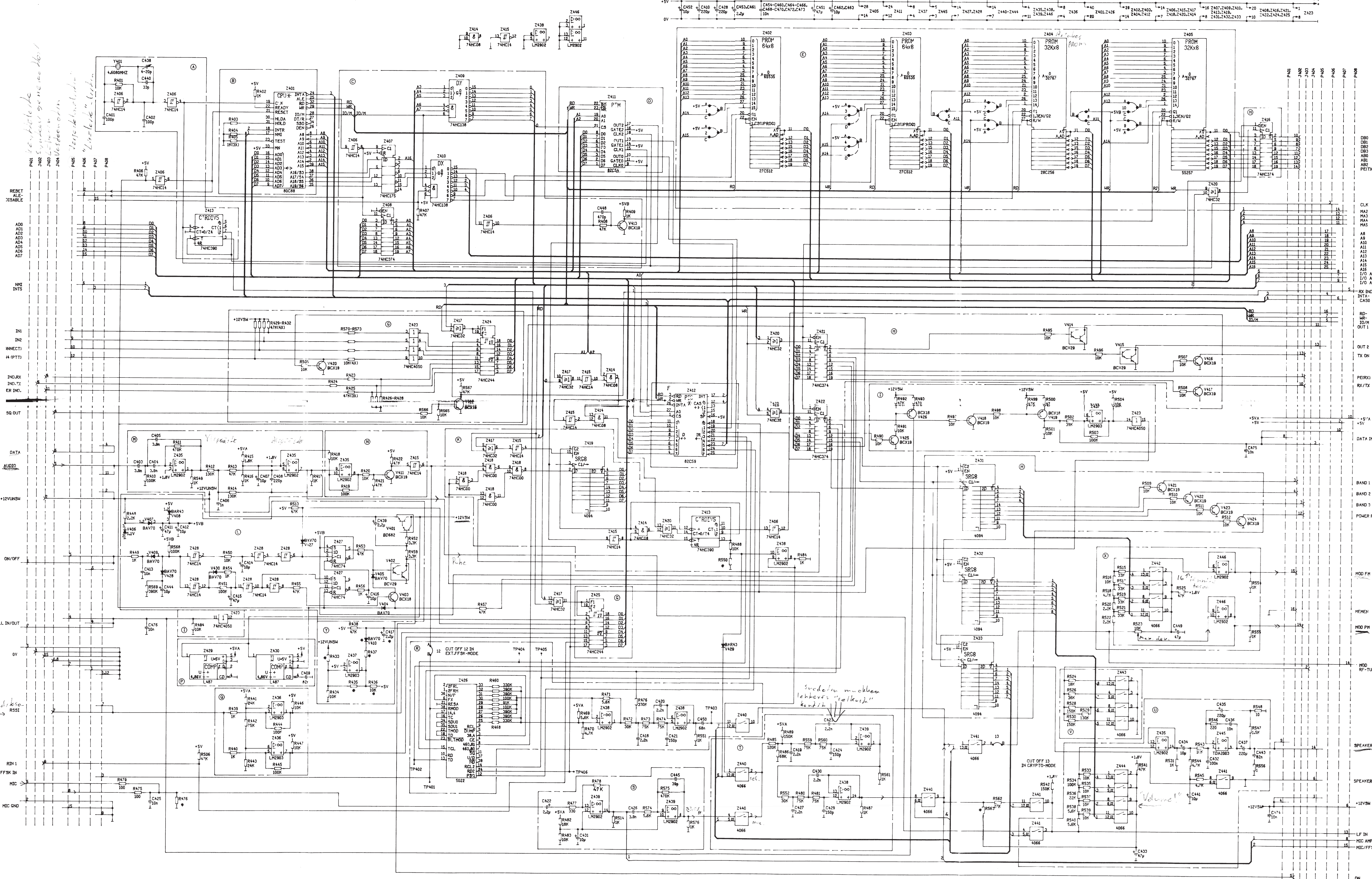


- A OSC/FREQ DIVIDER
- B CPU ADDRESS/DECODE
- C MEMORY
- D INTERRUPT CONTROLLER
- E INPUT INTERFACE
- F OUTPUT INTERFACE
- G SERIAL COMMUNICATION INTERFACE
- H TONE RECEIVER/TRANSMITTER
- I ON/OFF LOGIC
- M HP/F-P FILTER
- N SCHMITT TRIGGER
- O SV REGULATOR
- P RSST DECODER
- Q MEMORY
- R MIC AMP/LIMITER
- S T-PT TR
- T VPL/CONTR/SPEAKER AMPLIFIER
- U RF TUNING
- V MOD. SERVO COMPENSATION
- X LOW VOY TAGE INDICATOR
- Y NOT MOUNTED

- Z402 27CS12 ⇒ 1B-1C-2B-2C
- Z403 27CS12 ⇒ 3B-3C-4B-4C
- Z404 27CS12 ⇒ 5A-5B-6X-6Y-7B-7C
- Z405 27CS12 ⇒ 8A-8B-9X-9B-10C
- Z7C56,27C128,27C64 ⇒ 1B-1C-2A-2B
- Z7C56,27C128,27C64 ⇒ 3B-3C-4A-4B
- 8KRAN/EEPROM ⇒ 5A-5B-6A-6B-7C
- 8KRAN/EEPROM ⇒ 8B-8C-9B-9C-10B-10C
- 32KRAN/EEPROM ⇒ 3B-3D-4X-4Y
- 32KRAN/EEPROM ⇒ 5B-5C-6B-6C-7A-7B
- 32KRAN/EEPROM ⇒ 8B-8C-9B-9C-10A-10B



RESET
 ALE
 STABLE
 ADD
 AD1
 AD2
 AD3
 AD4
 AD5
 AD6
 AD7
 NMI
 INT5
 IN1
 IN2
 NNEXT1
 I4 (PTT)
 IND.RX
 IND.TX
 ER IND.
 SQ OUT
 DATA
 AUDIO
 +12VUNSH
 ON/OFF
 POLL IN/OUT
 OV
 RIN 1
 FFSK IN
 MIC
 MIC GND

DB0
 DB1
 DB2
 DB3
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